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THE APPLICATION OF AN HEDONIC MODEL TO A QUALITY ADJUSTED PRICE INDEX FOR COMPUTER PROCESSORS

City University of New York PH.D. 1986

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THE APPLICATION OF AN HEDONIC MODEL TO A QUALITY ADJUSTED PRICE INDEX FOR COMPUTER PROCESSORS

by

ELLEN R. DULBERGER

A dissertation submitted to the Graduate Faculty in Economics in partial fulfillment of the requirements for the degree of Doctor of Philosophy, The City University of New York.

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Introduction

Quality change presents difficult problems for economic measurement. The computing equipment industry is a case in point. Technological improvements have successively led to the introduction of new models of equipment with greater capabilities than existing ones. In the rapidly changing environment in which these products compete, price comparisons of equipment with the same quality required to construct meaningful price indexes are often not observed. Quality change prevents direct comparison of observed prices. In order for meaningful price comparisons to be made, quality must be held constant. This is a study of quality adjustment in prices of newly manufactured computer processors, one component of computing systems.[1]

Hedonic models, which have been used for many years and applied to many different products, provide one way to deal with the problem. The basic premise therein is that price differences across different units of transaction are due mainly to quality differences that can be measured in terms of common attributes, also called characteristics. An hedonic function, in effect, disaggregates transaction units into common characteristics.[2] Estimates of implicit (because they are not observed) characteristics' prices are derived from estimates of characteristics'

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[1]This study is part of a larger one at IBM in which hedonic equations were developed for three other types of computing equipment as well: auxiliary storage, printers, and displays. The quality adjusted price indexes estimated from these equations were used by the BEA in the recent revisions of the GNP accounts as described in Cartwright (1986).

[2]For a more complete discussion of hedonic functions as a disaggregator, see Triplett (1976).

coefficients. These implicit characteristics' prices are then used to estimate the price of an unobserved model by valuing its embodied characteristics.[3] In constructing a quality adjusted price index such estimates are then used for prices of models not transacted in the reference period.

The issues to be addressed in the application of an hedonic model to a quality adjusted price index for output of the computing equipment industry are as follows: (1) selection of the appropriate level of aggregation, (2) specification of the characteristics, (3) expansion of the hedonic model to deal with technologically induced price disequilibrium which occurs when models embodying new technology are sold at lower prices than existing ones because full market adjustment is not instantaneous.

Earlier studies have often shown the underlying theme of technologically induced price equilibrium, though none have explicitly dealt with its presence. In addition, all have suffered from the specification of characteristics which were either inadequate, or redundant, or both, and in some cases there has been a mismatch between included equipment and price.

This study will show that with the selection of appropriate performance characteristics, for which the equipment was designed and used, an

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[3]The formula for deriving the characteristics' prices from the estimated coefficients depends on the functional form of the estimated equation.

hedonic model expanded to deal with this phenomenon of technologically induced disequilibrium can be useful in estimating a quality adjusted price index for the output of computer processors.

Once estimated, such an index is useful in estimating real output. The Paasche-like index constructed in this paper declines at an average annual rate of 17.8% over the period 1972-1984. When this index was combined with analogous indexes estimated for storage devices, printers and displays, and used in the recent revisions by the BEA of the GNP accounts, it showed that an estimated 22.5% average annual growth in current dollar purchases of computing equipment represented a 42.5% average growth rate for constant dollar purchases.

Chapter 1 will describe the equipment under study and specification of characteristics as well as the meaning and role of technology as it affects market prices. Chapter 2 will develop the framework for the empirical work. In so doing, the traditional approach will be expanded to allow for the presence of technologically induced disequilibrium. The sample and empirical results will be discussed in chapter 3. The presence of technologically induced disequilibrium and the path of ensuing price adjustment will be examined. The best equation will be used to estimate the alternative quality adjusted price indexes explored next in chapter 4. Other hedonic studies of computing equipment will be considered in context.

CHAPTER 1

The object of analysis of this study is the computer processor, one component of a computing system. It is part of SIC 35731 and more narrowly defined as large and intermediate general purpose digital processors, at the seven digit SIC level, 3573106-3573109.

The Role of a Computer Processor in a Computing System

In order to gain perspective on the focus of the study and the characteristics selection, it is helpful to understand the components of a computing system in terms of their contribution to the system. A computing system is comprised of many component parts custom configured to meet a user's needs. Each component, also known as a box, provides a specialized service to the system. The activities of a computing system can be described briefly as follows: information is entered, instructions are executed, results are stored, and reports are generated.

Information is entered by hand (keying into a terminal) or by loading data and programs from machine readable magnetic tapes or disks. The computer processor, also called the CEC, houses the central processing unit (CPU), and main memory. The CPU executes instructions and the main memory stores the essential and most frequently used information so that it is available to the CPU. The memory hierarchy consists of a variety of boxes containing stored information that is available for

processing.[4] Closest to the CPU and an integral part of the CEC is the main memory. This is the fastest and most expensive part of the hierarchy; it holds programs and data most often required by the CPU for execution. The speed with which information is transferred to and from the CPU declines as one descends the hierarchy. The decline corresponds to the degree to which the components are mechanical, or electromechanical rather than electrical.

In addition to the contributions of these hardware components, computing system performance depends other things such as software.[5] System software falls into two main categories: operating systems which are general in nature and application programs which are specific.

Focus

The selection of system components rather than whole systems was based on two considerations. Keeping in mind that the goal is an output price index for newly manufactured products, we must examine the nature of the computing equipment industry's output to ensure a direct mapping between the selected unit of study and that output. The selected unit of study should be such that the valued sum of the units shipped equals the current value of industry shipments.

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[4]For a complete discussion of performance of large auxiliary storage, see Chen and Hodge (1986).

[5]See Bard and Sauer (1981) for a discussion of system performance modeling at IBM.

Newly manufactured computing equipment, SIC 3573, is comprised of components, not systems. Although data processing services are provided by the stock of computing systems, changes to that stock are often in the form of components which are used to modify existing configurations rather than to configure new whole systems. Total shipments of newly manufactured computing system components do not map into newly manufactured whole systems. This alone is sufficient reason to base the study on components rather than systems.

The second consideration is a practical one concerning the tractability of measurement of performance characteristics and the feasibility of measuring performance with the hedonic technique. At the component level, performance characteristics, of value to both producer and purchaser, are based on each component's role in the system. System performance, however, though driven to a large extent by the performance of individual hardware components, has the added dimension of component interactions. Systems get the work done through a network of component queues. Research, thus far, indicates that such analysis requires a more complicated technique than hedonics.

Specification of Characteristics

Effective disaggregation of any unit of output into its embodied characteristics requires that the selected characteristics provide a good representation of the unit in terms of what is valued by buyer and seller. In the event that measures of such characteristics of the final output are not available, it may be possible to use measures of characteristics of output at an earlier stage of manufacture as an approximation. The extent to which a good approximation may be made

depends on how directly the characteristics at the given stage of manufacture map in to characteristics of the final output. Of course, one must be sure not to select characteristics from different stages of manufacture to avoid redundacy. At any stage of manufacture, the selected characteristics must provide a complete representation of the product's capabilities.

The capabilities of a processor can be described in terms of speed with which instructions are executed and the capacity of main memory. Measurement of main memory capacity is straightforward and easily obtained (and uncontroversial). Megabytes, units of 1024 x 8, binary digits (0s or 1s) that can reside in main memory, are a readily acceptable measure of capacity.[6]

Speed, however, is an attribute more difficult to measure. Previous studies of computing equipment, some of which focused on processors and others on configured systems, have generally failed to include an adequate measure of processor speed. For example, Chow (1967), Stoneman (1976), and Archibald and Reece (1979), used as measures of processor speed, memory cycle time and the execution rate of a single instruction such as an addition or multiplication.

Such measures present two problems. Memory cycle time, a characteristic of an early stage of manufacture, is a poor approximation of processor

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[6]For a discussion of the conversion of information into binary digits and how computers work see Goldstine (1980).

speed. While in combination with other characteristics at the same stage, such as CPU cycle time, it has the potential to provide an adequate approximation of processor speed, alone it contributes only in a small way to the final output's capabilities- the speed with which all instructions are executed.[7] The other measure, the execution rate of one instruction, is a characteristic of final output (a different stage of manufacture) and it too is an inadequate proxy for the speed at which all instructions are executed. These two measures, at different stages of manufacture are redundant; memory cycle time contributes to the speed at which all instructions are executed. Together, they are wholly inadequate because they fail to provide a good approximation for processor speed.

Michael (1979), in apparent recognition of the inadequacy of the execution rate of an addition or multiplication (though easily obtained) as a measure of speed, devised dummy variables to capture other features believed to contribute to processor speed. Ratchford and Ford (1976) found that inadequate measurement of characteristics resulted in implausible coefficient estimates. This result led them to formulate a model for changes in price rather than the level.

There are two conditions which must be met in order for one instruction execution rate to represent all: (1) the processors being compared must have the same instruction sets and (2) the relative instruction

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[7] See Block and Galage (1978) for a first order approximation of the relationship of CPU and memory cycle time to the roles of executing instructions.

execution rates must not vary across processors. These conditions rarely hold.

A weighted composite of all the instruction execution rates for a typical job mix (or benchmark) is a better representation. A widely used measure of this kind is MIPS- millions of instruction executions per second, in which each instruction is weighted by its frequency of use in the job mix. However, two types of problems arise with the use of this measure. The first is comparability. If two processors have different instruction formats or different logic designs, their MIPS ratings will not be comparable. They can be made comparable as follows: Assume the MIPS rating of a given processor equals $MIPS_1$ and that N_1 equals the number of instruction executions in processing the job mix. If some other processor has a rating of $MIPS_2$ and its number of instruction executions equals N_2 for the same job mix, then the "equivalent MIPS" rating equals $MIPS_2(N_1/N_2)$.[8] The second problem relates to the choice of the job mix. It arises because of the difficulty of defining a truly representative benchmark. The advantage of equivalent MIPS as a measure of processor speed is realized only if the specified job mix is representative of the jobs expected to be performed by the processors being compared. Fisher, et al (1983) do make comparisons of price/MIP. It appears that lack of comparability prevented its further use in their study. Knight (1966) developed a measure similar in design to native or own MIPS (millions of own instructions per second), which were not comparable. To be assured of a

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[8]Discussion on this topic with Y. C. Chen has been most helpful.

consistent and comparable measure of speed, this study included IBM and plug-compatible processors for which equivalent MIPS are publicly available.

The Role of Technology

Technological improvements permit greater outputs to be produced with the same inputs. This has certainly been true for computer processors. The manufacture of processors with greater capabilities has been directly attributable to improvements in semiconductor technology. These improvements take the form of increased density, that is, packing more information (circuits) in the same physical space. Increased densities lead to greater capabilities because they shorten the distance electrons travel which means that more information can be stored, and instruction execution time is reduced.

Semiconductor chip density is used in this study to determine differences in embodied technology across processors. The number of kilobits residing on a single memory chip provides a means to compare the processors' embodied technologies. Though a chip is the most basic level of packaging, improvements in packaging at higher levels (cards and boards) have enabled improvements in manufacturing (and reduction in costs) to parallel chip density improvements. Embodied memory chip density is easily obtained and comparable. Unlike logic chips (whose proprietary nature prevents direct comparison), memory chips are a commodity in which the market gravitates to a new "best." It is understood that the use of memory chip density to represent logic technology as well is appropriate only to the extent that logic design is also improved by advances in semiconductor technology.

The impact of changes in technology over time has been to reduce quality adjusted prices. This time series phenomenon, by itself, however, need not require explicit treatment of technology in the hedonic framework. The need arises in individual cross-sections that are in a state of technologically induced price disequilibrium. When existing products are leapfrogged by products embodying a newer technology at a lower quality adjusted price, initially the marketplace is in a state of disequilibrium. This means that there is a period of time when two sets of prices for processors with the same characteristics coexist- one for products based on the old technology and one for those based on the new.

Explicit treatment of technology-induced disequilibrium is required in an hedonic function because failure to do so risks producing biased estimates of characteristics' coefficients. The potential for bias occurs because the forces causing the disequilibrium are likely to be correlated with the characteristics.

Fisher, McGowan and Greenwood (1983) recognized this problem and dealt with it by selecting only new models of one manufacturer (IBM), for inclusion in their analysis. It was assumed that such models embody the same level of technology and thus will be on the same hedonic surface. This made sense in their view because technological "leapfrogging" made each new announcement likely to move out the production possibility frontier (lowering the supply function) creating a new hedonic surface to be identified. Stoneman (1976) attempted to deal with the problem in another way. Generation dummies whose values were based on dates of introduction were intended to sort models by technology, that is, hold technology constant, while estimating the relationship between price and

characteristics. Michael (1979) noted the underlying theme in his own and other studies, of lower prices for newly introduced models, and it was suggested that the presence of multiple prices is related to the unavailability of new models. The BEA (1985), in its study, similarly found evidence of multiple frontiers producing multiple quality-adjusted prices. Statistical significance of the estimated coefficients on the "new" dummy in regressions of consecutive year pairs indicated that "new" models were sold at lower quality-adjusted prices than those which sold in the prior year as well.

No other study which included models embodying different technologies directly used information on those technologies to examine the presence of technologically induced disequilibrium, and the path of ensuing market adjustment using characteristics' coefficients estimated without risk of associated bias.

CHAPTER 2

Empirical Framework

An hedonic equation can be specified for a single cross-section in double log form as

$$(1)\quad \ln P_i = a + \sum b_k \ln X_{ki} + u_i$$

where

P_i price of the ith box

X_{ki} price of the quantity of the kth characteristic in the ith box

a intercept

u_i error associated with the ith box

The equation is expanded to incorporate pooled time series and cross-sections where changes in the intercept, that is, parallel shifts in the hedonic surface, are estimated over time by adding a dummy variable D_t for each year in the sample except one

$$(1a)\quad \ln P_{it} = a + \sum_{t}^{t-1} d_t D_t + \sum b_k \ln X_{ki} + u_i$$

The estimate of "a" represents the intercept for the year in which the time dummy was omitted, that is, the reference period. The estimates of

d_t represent the difference (or shift) between the surface in each base year t and the reference period.

Generally, to ease exposition, the omitted time dummy is the first sample year so that estimates of d_t permit convenient comparisons of the shift in the hedonic surface through time. Other studies of computing equipment have produced estimates of d_t which are negative and generally increase in magnitude over time. These negative price changes, holding quality constant have been attributed to technological change.

In order for the time dummies of (1a) to successfully capture technology driven price reductions, and to avoid the possibility of technology associated bias in the estimated characteristics' coefficients, one of two conditions must hold within any time period t: all products transacted in the same time period embody the same level of technology, or, in the absence of immediate (total) diffusion of new technology, prices of products embodying older technologies adjust fully and instantaneously resulting in one prevailing quality-adjusted price for all products (regardless of differences in embodied technologies). To directly test for the failure of either condition (1a) will be expanded to allow for nonquality associated price differences to be present. This requires grouping the processors in the sample into classes according to their embodied technology within each period. These technology classes enter the equation as follows:

$$(2) \quad \ln P_{it} = a + \sum^{t-1} d_t D_t + \sum^{m-1} c_{mt} T_m D_t + \sum b_k \ln X_{ki} + u_i$$

where T_m denotes a dummy variable for the m^{th} technology class

and $T_m D_t$ denotes a dummy variable for the m^{th} technology class in the t^{th} period. There will be (m-1) t such variables.

In the event that only one technology class is present (m=1) the technology class by time dummies will not enter the equation (m-1=0). If m-1 classes are present in period t but are embodied in products which compete at the same quality-adjusted price then the dummies will enter the equation but their coefficients c_{mt} will not differ from zero indicating that all m classes have quality-adjusted prices not different from that of the omitted class in the same year.

For convenience of exposition, the time dummies will enter for each period except the earliest covered by the sample, making that the reference year. In so doing the d_t estimates provide direct comparison between each year t and the first year in the sample. To facilitate the investigation of technologically induced price disequilibrium, in each year the technology class dummy chosen for omission will correspond to the "best" available (as will be described in the section on specification of characteristics and technology). Omitting the "best" technology class each year means that each c_{mt} represents the estimated difference in price, given quality (that is, holding characteristics quantities constant) between the group of models embodying each "nonbest" technology as compared with the group embodying the "best." The empirical work will be conducted as follows: Equations (1a) and (2)

will be estimated and compared to assess the contribution of technological stratification. Intra-year comparisons of coefficients across technology classes each year will be tested for statistical difference with each other. Equation (2'), a simplified version of (2) with two kinds of restrictions will be estimated. First, technology class coefficients not different from zero (that is, not priced differently from the best) are restricted to be zero by dropping them out of the equation. Second, technology class coefficients not different from one another are restricted to be equal by collapsing those technology class dummies into one variable. Equation (2') and (2) will be compared to test the validity of the restrictions as a group. An alternative to (2) and (2') will be estimated where $\sum d_t D_t$ and $\sum c_{mt} T_m D_t$ are replaced by a set of 3 technology variables in attempt to directly measure technology associated cross-section and time differences. Corresponding equations will be estimated for each cross-section underlying (2') and the set of single year regression compared with pooled equation (2') to confirm the constancy of b_k over time. Box-Cox transformations will be used on pooled (2') to test for the best functional form.

CHAPTER 3

EMPIRICAL WORK

Sample

Characteristics and purchase prices covering the years 1972-1984 were collected for a total of 67 boxes sold by 4 vendors. Characteristics were obtained for compilations published in COMPUTERWORLD and DATAMATION. The data were augmented by reports of new product announcements in the general and trade press. Estimates of 370 equivalent MIPS are publicly available for processors produced by IBM and plug-compatible manufacturers. MIPS ratings published for the processors of other manufacturers may not be equivalent. The published data are unclear on this matter. This problem imposed a constraint on sample size. A reduced sample was accepted to enable the use of a comparable, and, in principle, superior measure of speed in order to avoid the bias created by measurement error.

This study included large and intermediate general purpose processors. It also excludes small processors because they are typically packaged with auxiliary storage devices (disk drives or cassettes) under the covers. Estimates of their performance must account for component queues.

Typically, manufacturers make each CPU available with a choice of main memory capacities which are available in increments. Since there was no means by which to determine a typical main memory capacity, two models of each processor were included in the sample. Prices were obtained for two main memory capacities: one increment greater than the minimum

offered, and the maximum. Implementing these memory size rules often meant changes in memory size over time for the same CPU, and the values for the characteristic were changed accordingly in the data set in the next calendar year. Prices for IBM products were taken from historical sales manuals. Other manufacturers' prices were derived from price information in press articles. Base prices for processors with minimum memory, memory increment size and price, and maximum capacity available were used to calculate values for included main memory capacity and corresponding prices. Annual prices were created by weighting together different prices within a year by their respective duration. No reports of price change were treated as no price change.

In principle, a model should remain in the sample as long as it was in new production. However, volume of shipments data for each processor model are unavailable. Quantities shipped in each sample year were estimated from the year to year changes in IDC's annual tabulation of installed general purpose computing systems in the U.S., published in EDP reports.[9]

A model was included in the sample for each year that the stock of its installed equipment increased. It was assumed to be in new production during those years because an increase means that new shipments exceeded the sum of customer returns of leased equipment and retirements. A decrease indicates that the converse was true and it was more likely

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[9]CECs could be identified because systems are known by their CEC model name (or number).

that shipments, if any, were comprised of recycled equipment manufactured in a prior year.[10] A model entered the sample the first year it appeared in the stock and was deleted the year after its stock peaked.

Small sample size and poor quality shipments data present serious limitations to the data set. Neither, however, in the author's view could have been avoided. As noted earlier, when faced with the choice of a large sample or adequate measure of speed, better measurement was selected.

The year 1972 was chosen to begin the sample period for two reasons. The introduction of semiconductor main memory in 1971 made it practical for the first time to house logic and main memory under the same cover, and henceforth was called the processor or the CEC (central electronic complex). The CEC together with minimum required gear from then on comprised a basic transaction unit.

By 1972, outright purchase overtook lease arrangements as the dominant mode of equipment acquisition. Purchase prices are preferred to lease prices for the purpose of this study because when multiplied by the number of units shipped they yield the current value of shipments, the series for which a quality-adjusted price index is desired. Though transaction prices would be preferred, they were not available, imposing

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[10] Even if IDC stocks were accurate, returns of leased equipment will cause a downward bias in the shipments estimates derived this way. There is no publicly available alternative.

the use of manufacturer's list prices. The severity of this problem depends on the degree to which transactions occur at unpublished discounted prices.

Empirical Results

Equation (1a), the traditional hedonic equation with price as a function of characteristics and time dummy variables for each but one year, was estimated for the full sample period, denoted 1 in Table 1. The results indicate that, in accord with prior expectations, MIPS and main memory both contribute directly and significantly to the price of processors. Speed is shown to be by far the dominant characteristic. It should be. After all, the role of processors is to execute instructions.

To investigate the matter of technologically induced disequilibrium, dummy variables were defined for models in each technology class each year as detailed in Table 2. The density of magnetic core memories (which are not chip-based) which were present in the sample only in 1972 required approximation. One additional distinction was made in 1973, the only sample year in which two different types of semiconductors memory with the same density were both present. This final sort was made because the two types of semiconductors, bipolar and FET, differ greatly in price and circuit speed.

An explicit test of technology induced disequilibrium was made with the introduction of these technology class-by-year dummy variables (for each but one technology class), for each but one year in the sample. For example, one such dummy for technology class 8 in 1980 is assigned a value of one for all processors embodying 64k memory chips in the year

1980 and zeroes for all other processors and all other years. For convenience of exposition, the omitted technology class was that of the "best", defined as the densest. The omitted year was 1972. This means that, for any given year, estimated coefficients on the technology class dummies for that year represent (in log form) price differences between each of those classes and the "best." Furthermore, the combined effect of omitting the 1972 time dummy and the best technology class in each year means that the estimated coefficient of each time dummy represents the price difference between the "best" technology in that year as compared with the "best" in 1972.

Comparison of Equation (2) with Equation (1a) in Table 1 indicate that technological stratification reduces the standard error of estimate substantially. The following F test of the nested hypothesis confirms the significance of the improvement made by the addition of the technology by year dummies.

TABLE 1

REGRESSION COEFFICIENTS: 1972-84 POOLED REGRESSIONS

	1		2		2'	
CHARACTERISTICS	COEFF.	t VALUE	COEFF.	t VALUE	COEFF.	t VALUE
Speed	.798	(35.1)	.780	(39.0)	.783	(41.4)
Capacity	.173	(6.6)	.219	(10.0)	.215	(10.1)
INTERCEPT	7.578	(94.1)	7.945	(79.1)	7.944	(79.5)
DUMMIES						
Year dummies	*		*		*	
Tech. class by year			*		*	
R^2	.953		.953		.973	
MEAN SQUARE ERROR	.062		.039		.038	
SAMPLE SIZE	296		296		296	

°Dependent and independent variables, except dummies, are in natural logarithms. An asterisk denotes set of dummies included in regressions.

TABLE 2

PROCESSOR MAIN MEMORY TECHNOLOGIES 1972-1984

CLASS CODE	MATERIAL	TYPE	MEMORY CHIP DENSITY (KILOBITS) PER CHIP)	YEARS IN SAMPLE	YEARS "BEST"
1	Magnetic Core		.0025*	1972	
2	Semiconductor	Bipolar	.125	1972	1972
3	Semiconductor	Bipolar	1	1973-74	
4	Semiconductor	FET	1	1973,76-79	1973
5	Semiconductor	FET	2	1974-83	1974
6	Semiconductor	FET	4	1975-82	1975-78
7	Semiconductor	FET	16	1981-84	
8	Semiconductor	FET	64	1979-84	1979-84

*Estimated using relative volume/megabyte from Pugh et al. Table 1.

Ho: The addition of technology stratification dummies does not add to the explanatory power of the simple model.

$$F = \frac{R_Q^2 - R_K^2}{1-R_Q^2} \cdot \frac{n - Q}{Q - K} = \frac{.9727-.9525}{1-.9727} \cdot \frac{257}{24} = 7.9$$

CRITICAL VALUE 1% LEVEL = 2.21

5% LEVEL = 1.73

Reject null hypothesis. Accept Equation 2 in preference to Equation 1a.

Table 3a displays the estimated technology and time differences of Equation 2. Upon examination by row of these coefficients and their t statistics it appears that in seven cases the prices of nonbest technology classes may not be significantly different from the best (zero) within the same year. Furthermore, there are 4 cases where nonbest technology classes though different from the "best," do not appear to be different from one another.

A formal test for statistical difference between two coefficients is $t_{n-k} \sim \frac{\hat{B}_i - \hat{B}_j}{S^2_{\hat{B}_i} + S^2_{\hat{B}_j} - 2 (\text{est cov } \hat{B}_i \hat{B}_j)}$ and yields, as shown in Table 4, the following results for computing "nonbest" technologies.

TABLE 3a

Equation 2

Regression Coefficients on Technology Class-by-Year Dummies

YEAR	"BEST"	Technology Class 1	2	3	4	5	6	7	8
1972		0.554							
		(-4.4)	*						
1973	-.239			0.295	*				
	(-1.8)			(2.3)					
1974	-.195			.284		*			
	(-1.6)			(2.3)					
1975	-.746					0.524	*		
	(-4.3)					(3.3)			
1976	-.798				0.160	.557	*		
	(-4.6)				(.8)	(3.5)			
1977	-1.003				.318	.383	*		
	(-7.5)				(2.4)	(3.0)			
1978	-1.245				.379	-.084	*		
	(-9.3)				(2.9)	(-.7)			
1979	-2.283				1.181	.877	0.833		*
	(-13.1)				(6.0)	(5.4)	(5.3)		
1980	-2.257					.537	.544		*
	(-16.7)					(4.6)	(5.3)		
1981	-2.167					.262	-.038	0.327	*
	(-17.7)					(2.7)	(-.4)	(3.7)	
1982	2.293					.147	.142	.281	*
	(-19.0)					(1.0)	(1.6)	(3.7)	
1983	-2.392					.173		.032	*
	(-20.3)					(1.2)		(.4)	
1984	-2.554							-.050	*
	(-21.0)							(-.8)	

TABLE 3b

Equation 2'

YEAR	"BEST"	Technology Class 1	2	3	4	5	6	7	8
1972		-.554	*						
		(-4.4)							
1973	-.235			.293	*				
	(-1.8)			(2.3)					
1974	-.192			.282		*			
	(-1.6)			(2.3)					
1975	-.743					.524	*		
	(-4.3)					(3.3)			
1976	-.715				0	.477	*		
	(-5.1)					(4.0)			
1977	-.997				.318	.383	*		
	(-7.5)				(2.5)	(3.0)			
1978	-1.282				.420	0	*		
	-10.7)				(3.6)				
1979	-2.276				1.179	.877	0.833		*
	(-13.1)				(6.0)	(5.5)	(5.3)		
1980	-2.250					.539	.539		*
	(-16.8)					(5.7)	(5.7)		
1981	-2.172					.273	0	.338	*
	(-18.5)					(3.0)		(4.1)	
1982	2.248					0	0	.243	*
	(-19.3)							(3.4)	
1983	-2.273					0		0	*
	(-20.5)								
1984	-2.564							0	*
	(-21.8)								

TABLE 3c

Price Indexes by Technology Class
(1972 "Best" = 100)

YEAR	"BEST"	Technology Class 1	2	3	4	5	6	7	8	9
1972	100.0	57.5	100.0							
1973	79.0			106.0	79.0					
1974	82.5		109.4			82.5				
1975	47.6					80.3	47.6			
1976	48.9				48.9	78.8	48.9			
1977	36.9				50.7	54.1	36.9			
1978	27.7				42.2	27.7	27.7			
1979	.103				33.3	24.6	23.6		10.2	
1980	10.5					18.1	18.1		10.5	
1981	11.4					15.0	11.4	16.0	11.4	
1982	10.6					10.6	10.6	13.5	10.6	
1983	10.3					10.3		10.3	10.3	
1984	7.7							7.7	7.7	

TABLE 4

TESTS FOR INTRAYEAR DIFFERENCES ACROSS TECHNOLOGY CLASSES

YEAR	CLASS CODES	$\frac{\hat{B}_i - \hat{B}_j}{S_{\hat{B}i} + S_{\hat{B}j} - 2(\text{est cov } \hat{B}_i \hat{B}_j)}$	$\sim t$	RESULT
1977	4,5	$\frac{.318-.383}{(.127)^2+(.127)^2-2(.006)}$	= -3.1	different
1979	4,5	$\frac{1.182-.876}{(.197)^2+(.161)^2-2(.010)}$	= 6.8	different
	5,6	$\frac{.876-.831}{(.161)^2+(.156)^2-2(.020)}$	= -4.4	different
1980	5,6	$\frac{.535-.541}{(.115)^2+(.101)^2-2(.007)}$	= -.6	not different
1981	5,7	$\frac{.260-.326}{(.097)^2+(.088)^2-2(.003)}$	= -5.9	different
1982	6,7	$\frac{.142-.282}{(.091)^2+(.075)^2-2(.002)}$	= -14.1	different

In three cases occurring in 1977, 1979, and 1980, two nonbest technologies are embodied in processors not priced differently from one another, (holding characteristics constant). Equation (2'), a simplified form of Equation (2), in which the restrictions suggested by formal tests of statistical differences between coefficients in Equation (2), was estimated next. The estimated time and technology class coefficients are displayed in Table 3b.

Although, the restrictions were indicated as the result of individual t tests, it is further necessary to test the validity of the restrictions as a group. An F test comparing Equation (2) with nested Equation (2') enables one to reject the null hypothesis that they are different.

Ho: Restrictions to Equation 2 do not reduce explanatory power of fully unrestricted equation.

$$F = \frac{.9727 - .9719}{1-.9727} \cdot \frac{257}{11} = 0.7$$

CRITICAL VALUE 1% LEVEL = 3.6
5% LEVEL = 2.4

In other words, we are entitled to implement the restrictions and proceed to examine equation 2' with direct focus on significant technology associated price differences appearing in the lower left panel of Table 3.

Inspection by row reveals that in all cases but one, that is, class code 1 in 1972, products embodying nonbest technologies have quality adjusted prices higher than or equal to those competing products embodying the best in current production. The odd case occurring in 1972 concerns memories made from magnetic core, a material which had been in

production at least since 1955. Although core memory, over its production life, experienced great improvements in densities and cost reductions by 1972, though relatively inexpensive to continue production, further improvements in density and cost were unlikely. The future belonged to semiconductors. In all other cases, newer technology meant lower quality adjusted prices.

The estimated time and technology class dummy coefficients from 2' are used to derive price indexes for each technology class as shown in Table 3c. Arbitrarily setting the value for technology class 2 in 1972 to 100, all values in this panel are relative to this class. Equal index numbers within a year represent technology classes priced alike. Intra year differences indicate multiple price regimes.

As the estimated 1972 price difference indicates, semiconductors were initially expensive. It may be that the enormous reduction in size permitted consumer tolerance of such a premium. By 1975, however, 4 kilobit FET chips, enabled processor prices to be 15% lower than those embodying core in 1972.[11] Furthermore, the manufacture of processors with empty slots to permit future insertion of additional memory (and logic) indicated that once in the world of semiconductors floorspace reductions were not considered important.

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[11]The estimated price difference between processors embodying FET 2k chips in 1975 and those with core memories in 1972 is taken as the antilog of the difference between the estimated coefficients, $e^{-.715-(-.554)} = .850$.

Inspection by column reveals that over time, with one exception -- technology class 4, the estimated price differentials between "nonbest" and each prevailing "best" technology continually erode. The introduction of a new "best" initially shows high estimated price differentials which again erode with time. Prices of products embodying older technologies are cut or production ceases, that is, the technology class drops out of the sample.

Technology class code 5, representing the 2 kilobit FET chip, has the longest life -- 10 years. It is "best" only in its year of introduction, 1974, and over the next four years becomes fully competitive in price with the "new best," the denser 4k FET technology (class code 6).[12] In 1979, yet another "best" is introduced and once again, with successive price reductions, technology class 5 becomes fully competitive and remains so through 1983, its last year in production.

The prices of technology classes 6 and 7 become fully competitive and remain so until further price reductions of the best drive them from production.

Technology class 4 is peculiar. First introduced in 1973, it is "best" only in that year, and is substantially less expensive than its only

[12]The continued ability of the FET 2k technology class to incur price reductions may seem in part from the fact that in the sample, only IBM processors embody this technology and IBM's packaging is said to have enabled the 2k chip to be as effective as a 16k chip. For a discussion of packaging at IBM, see Seraphim and Feinberg (1981).

competitor. However, after just one year it is no longer in production and is replaced by a new "best", in 1974 shipments of the same models. It is reintroduced in 1976, this time embodied in new processors at prices fully competitive with the current best, class 6. Subsequently, although this class did sustain price cuts, it continually lost ground (that is, its price differential with "best" increased) through 1979, its last year in manufacture. As expected, though, shipments declined because prices did not reflecting reduced demand for models with reduced price competitiveness.

Equation 2' interestingly reveals that although 8 of the 13 sample years contain products embodying at least 3 different technologies, 5 of those years indicate the presence of only 2 price regimes. This means that for the most part, products embodying "nonbest" technologies are, priced alike or priced like the "best." Two years, 1983 and 1984 are found to be in equilibrium. In 1977, 1979 and 1981, there are more than 2 coexistent quality adjusted prices -- a finding to be investigated.

In 1977, although processors embodying each of the 2 classes of nonbest technologies did sustain competitive price cuts, the regression results indicate that they are not quite priced alike. The less dense class code 4, lost competitiveness vis-a-vis the best (class 6) while technology class 5 gained. The estimated price differential is a small 6.8% (though statistically significant). Though not alike, the two nonbest classes are priced closely, and both are expensive relative to the best.

In 1979, the findings indicate the presence of four price regimes. This was the last year of production of products embodying the FET 1k chip (technology class 4). Few transactions took place that year which is not surprising, because, quantity should adjust (due to reduced demand) when prices do not.[13] The other competing nonbest technologies are priced very much alike with an estimated 4.5% difference which is not very meaningful though statistically significant. Again, though processors in all classes underwent price reductions from their prior level, those embodying nonbest technologies were not able to immediately match the prices of the spanking new best.

The finding that three different quality adjusted prices were present in 1981 may be related to a sample phenomenon. This is the only example of a first time introduction of a new technology that is not the "best" technology, technology class 7. Furthermore, stratification indicated that the difference in its quality adjusted price relative to another FET 2k, "nonbest" was a small, 6.7%, although, significant. Successive price cuts did improve the 16k chip's product competitiveness and by 1983 this class had met fully the 64k challenge (class 8).

The last two years in the sample, 1983 and 1984 are found to be in equilibrium. The movement to full equilibrium from 1982 to 1983, Only

[13]The only processor still shipped in 1979 with FET 1k technology was 3138 manufactured by IBM. While it may be suggested that the premium is likely to be overstated because it reflects the 3138's list price premium relative to the best that year and that transaction prices would surely have been lower, this is not the case, IBM did not discount 3138s.

three of the four classes present in 1982 continued in production the following year. In 1984 equilibrium was maintained but this time products embodied only two surviving classes.

The results support the view that technological improvements induce disequilibrium, the market does adjust and the period of adjustment is longer than one year.[14]

It should be emphasized that technological improvements need not have resulted in transactions at more than one quality adjusted price. Transactions in multiple price regimes (reflecting technologically associated cost differences) could only occur when matched by consumers' tolerance of the differences. Consumer intolerance of the inability of producers to offer fully competitive prices on models embodying older technologies would result in a full adjustment in quantity (disappearance of higher priced models embodying older technologies) and transactions would be observed at only one quality adjusted price -- the "best."

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[14]It has been suggested that the finding that products embodying new technologies are initially cheaper may be due in part to unbundling -- the pricing of fewer different characteristics together as a unit, especially likely with the introduction of the 4341 by IBM in 1979 which was the first processor to embody 64k memory chips. If this were the case, one would expect the estimated premiums of competing "nonbest" technologies to persist and never be driven to zero. The finding that in most cases, prices of products embodying older technologies do become fully competitive is evidence that unbundling does not refute the interpretation of the finding given here.

A puzzle which still remains is why manufacturers do not do one of the following: raise the quality adjusted prices of the new models in limited supply equal those widely available or make the new models widely available right away. One possibility is that the offering of new models at low prices is a way of disseminating information about the impact of the new technology.

Further Testing

Pooling of Cross Sections

Thus far, the results presented have been estimated using pooled time series and cross section data. While pooling provides an obvious convenience, it is necessary to test whether it is appropriate. Selecting Equation 2' for further testing, individual cross section equations were estimated for each of the thirteen sample years which when combined yield the full regression. These equations are shown in the Appendix (p. 60).

The results indicate that for all thirteen cross sections MIPS and main memory are significant and furthermore, t statistics on technology dummies support all of the restrictions in the full pooled equation. The following F test result supports the null hypothesis that the errors in the single equations come from same population as the full multiyear equation. This means that the characteristics coefficients are constant over time; the contour of the hedonic surface does not change over time, it experiences parallel shifts resulting from technological change. It should be noted that constant characteristics coefficients do not imply constant characteristics prices. Continued use of the pooled sample is based on this finding.

Ho: SSE from single year equations do not come from a different population as pooled time series cross sections.

$$F = \frac{(SSE - SSE_S)/K}{SSE_S/(n-K)_S} = \frac{10.234-7.929}{7.929} \quad \frac{28}{296-50} = .04$$

CRITICAL VALUE 1% LEVEL = 2.01
5% LEVEL = 1.62

Functional Form

Box-Cox transformations were used to enable comparison of three alternative functional forms.[15] Their transformation is defined as

$$y = \frac{y^{\lambda} - 1}{\lambda} \qquad \lambda \neq 0$$

$$= \log y \qquad = 0$$

This transformation is advantageous because it permits direct comparison of the residual sum of squares, and hence standard error of estimate. In addition to the double log form, two alternatives were tested. The results are shown in Table 5. A semilog equation, where $\lambda = 1$ for price and 0 for characteristics was estimated and proved to be inferior to the double log form. The third form set $\lambda = 1$ for both dependent and independent variables.[16]

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[15] For a description of Box-Cox transformations see Maddala (1979) p. 315-317.

[16] A range of alternatives were examined where was varied from 0 to 1 in increments of .1 for the dependent variable independently from both characteristics. (λ was not varied independently for each characteristic). The lowest standard error of estimate was .027 which resulted from $\lambda = 0$ for price $\lambda = .3$ for characteristics. This is so close to double log that my preference for simplicity combined with my a priori expectation that the function would be double log led me to chose from the three alternatives shown in Table 5.

TABLE 5

ALTERNATIVE FUNCTIONAL FORMS

FUNCTIONAL FORM	STANDARD OF ERROR OF ESTIMATE
ln (price) = f (ln MIPS, ln MEM)	.038
ln (price) = f (MIPS, MEM)	.198
price = f (MIPS, MEM)	.610

On the basis of lowest comparable standard error of estimate, the double log specification is accepted as preferred.

Linear Homogeneity

It is interesting to note that Equation 2 and 2' appear to be linear homogeneous functions of price with respect to characteristics. A formal test of linear homogeneity of Equation 2' in the form of a restriction yields coefficients of .783 on ln MIPS and .217 on ln memory, with an insignificant t = -0.2 on the restriction (see appendix). The implication of this finding is intuitively pleasing, that is, a doubling of characteristics leads to a doubling of price; for any given technology, at any point in time, doubling processors characteristics will double its price. Moreover, a valuation of the characteristics yields the box price.

Memory Size Rule

Since the sample includes CECs with two different memory sizes for each CPU, it is necessary to test whether the characteristics' coefficients are affected by included main memory capacity rules. Adding two additional variables to Equation 2' permits such a test. A dummy variable is defined representing those CECs with minimum plus one increment of memory with a value of "1" for all CECs with minimum plus one increment of memory and a value of "0" for those with maximum. Then two variables are defined representing ln MIPS and ln memory of CECs with minimum plus one increment of memory, by multiplying this dummy variable by ln MIPS and ln main memory previously used. Adding these two variables to Equation 2' and reestimating will provide estimates of the difference between each characteristic's coefficient for those CECs

that include minimum plus one increment of memory, with the entire sample. The coefficients (t statistics) on these differences are .019 (0.5) on ln MIPS and -.012 (-0.4) on ln main memory indicating no significant difference in the estimated characteristic coefficients between the one memory size and the entire sample.[17]

Technologically Associated Coefficient Bias

To address the question of biased estimates of characteristics coefficients when failing to account for the presence of technologically induced price disequilibrium, a standard t test is used to compare each characteristic's estimated coefficient between the tradition Equation 1 and fully expanded Equation 2. For ln MIPS and ln Memory, the t statistics equal 20.0 and 39.4 respectively. These results indicate a significant difference at the 1% level. We can conclude from this that failure to account for this phenomenon does result in biased characteristics' coefficients estimates.

Alternative Expansion of Equation 1a to Account for Technology

An alternative use of the information on technology used to sort the CECs into technology classes is in the form of direct measures. From Table 6 three variables are used to define candidates which are

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[17] It has been suggested that the smallness of the sample, which contributes to the finding that the individual cross-sections can be pooled, is in part due to the failure to include a model for every main memory size available with a CPU. Whether or not such additional observations would contribute in a meaningful way is answered at least, in part, by this test. The arbitrary selection of the memory sizes included in the sample differ in range by model, and over time. The finding that the characteristic coefficients do not differ suggests that

(Footnote Continued)

TABLE 6

COMPARISONS OF ALTERNATIVE EXPANDED EQUATIONS

DEPENDENT VARIABLE: ln(PRICE/FWPGNP)*

	EQUATIONS		
	2	2'	3
CONST	8.062	8.061	7.976
	(80.3)	(81.0)	(86.8)
ln(MIPS)	.780	.783	.757
	(39.0)	(41.7)	(20.8)
ln(MEM)	.219	.215	.128
	(10.0)	(10.2)	(3.035)
OWN TECHNOLOGY			-1.65
			(5.8)
AGE			-.091
			(5.1)
BEST			-.384
			(-11.2)
TIME & AGE DUMMIES	*	*	--
MSE	.039	.038	.159
R^2	.973	.972	.874
F	240.7	343.4	400.6

*FWPGNP = Fixed Weight GNP Deflator

(Footnote Continued)
additional observations would not alter the results and would be an artificial way to increase sample size.

intended to capture both the cross-sectional price differences and time associated price changes resulting from the impact of technology.

"Own" technology is defined by assigning to it the value of its embodied memory chip density under the basic assumption that technology associated production cost differences will show up in price. However, since experience in production and expected obsolescence over the life of a processor can also be expected to affect prices, an "age" of own technology variable is needed as well. It is defined simply as the number of years since the embodied memory technology first appeared in a processor. A third technology variable to capture the competitive pressure on price exerted by technologically superior substitute is included and is measured by the density of the best technology available each year. It does not vary within each cross section.

Consideration of the set of technology variables as a replacement for the technology and time dummies of Equation 2 and 2', does not require a prior assumption of multiple price regimes. It is possible for age-related reductions in costs of production to permit products embodying older technologies to be fully price competitive with newer ones for some period of time, (that is, until the newer technologies age-related cost reductions make it impossible for the older ones to compete).

Before the set of technology variables is tested as an alternative to the technology class dummies in Equation 2 and 2' it must be recognized that over time, at most they can be expected to account for is technology associated price changes, and not price changes associated

with changes in the general price level. Furthermore, one can expect that the time series effect of technology would be collinear with a set of traditional time dummies. If the regression could be estimated with both technology variables and time dummies then the former would be expected to capture the technology effect and the time dummies' estimated coefficients would be small and positive reflecting changes in the price level.

One possible empirical specification, which can be estimated, accounts for the general price level effect by dividing the dependent variable by a fixed weighted private GNP deflator and then estimating Equation 3. The new dependent variable is a function of characteristics and the three technology variables. The "best" technology variable is entered as a weighted average of "best" in the current year and the prior year to allow for continued competitive impact over two years. Comparing standard errors of estimate indicates that Equation 3 does not fully capture the technology and time effects of Equations 2, and 2'. For purpose of comparison, Equation 2 and 2' (see appendix) are reestimated with the same independent variable as Equation 3 and are compared in Table 6.[18]

[18]Note that the characteristics' coefficients will not differ with the new dependent variable for Equations 2 and 2'. This is because the deflator varies over time but not in the cross section and all the cross section variation not captured by the coefficients is captured by the technology class by year dummies. The only coefficients that can be affected, therefore, are the time dummies and constant and they will differ exactly by the ln of the deflator.

The failure of the direct measures of technology reflects, in good part, the inability of memory chip density to summarize logic technology as well as that of main memory. Although greater speeds as well as capacities have been achieved by packaging increased numbers of circuits together, this measure fails to adequately summarize all the technological improvements of both.[19]

Plausibility of Findings

The willingness of sellers to offer products embodying older technologies at higher quality adjusted prices than those embodying newer ones (as production costs dictate) makes sense. However, in order for transactions to occur at more than one quality adjusted price, buyers must be willing to pay such a price difference. Why would they and why would their willingness be related to memory chip density or any direct measure of technology?[20]

At the time of their introduction, processors embodying new technology are limited in supply.[21] Over the life cycle of a product (also called product cycle), availability increases in subsequent years and then declines as manufacturers gear up production of the successors. To the extent that the newer products are not widely available, one can view

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[19]It is also possible that for logic, the chip is not the appropriate level of packaging to investigate density. Higher levels of packaging such as boards or modules may be more appropriate. See Rymaszewski et al (1981) p 606.

[20]Discussion on the topic with Zvi Griliches has been most helpful.

[21]This limited supply of new models phenomenon was noted in Michael (1979).

the premium on older products with the same capabilities, as the price of immediate delivery. It has also been suggested that there is uncertainty or a lack of information regarding how "good" the new products really are. Until information on what can they really do is available, it is possible that the older products which are "known" could command a premium.

In answer to the second part of the question, the direct measures of technology, own embodied technology and its age, need not be directly related to all consumers willingness to pay a price differential and yet might be to some. If we assume a competitive marketplace in which producers offer the lowest price possible, then transactions will occur at those supply prices or not at all. If buyers consider the premiums too high and the manufacturers cannot lower them, then transactions will not occur and buyers who cannot get the newer products now will wait for them to become available. In this sense, the premiums only indicate the behavior of some buyers. Others have effected a quantity adjustment when it failed to occur sufficiently in price.

Characteristics Prices

Estimated characteristics prices for processors as shown in Table 7 are calculated as follows. the price of the kth characteristic in year t, denoted P_{kt} is estimated as

$$\hat{P}_{kt} = \frac{\delta P_t}{\delta x_k} = b_k \sum_m \left(\frac{\bar{P}_{imt}}{\bar{x}_{ki}} \right) v_{mt} ,$$

where the overbar denotes the arithmetic mean; P_{imt} denotes the price of the ith model of the mth technology class in year t; x_{ki} denotes the

quantity of the kth characteristic in the ith model; v_{mt} denotes the share of characteristics from the mth technology class shipped in year t; and b_k denotes the regression coefficient for the kth characteristic.

The characteristics prices, as estimated from Equation II' are shown in Table 6. These estimates are partial derivatives; they are stated as the price of speed holding everything else constant (including memory) and the price of memory, cet par (including speed).

The prices of both characteristics have fallen dramatically over the period 1972-1984. As Table 7 indicates, the price of speed in 1984 is approximately 1/8 of its price in 1972. The price of memory is approximately 1/20.

TABLE 7

Estimated Characteristics' Prices
(Thousand Dollars per Unit)

Year	Speed, in MIPS	Capacity, in Megabytes
1972	1,801	497
1973	2,293	404
1974	1,906	332
1975	1,827	283
1976	1,821	285
1977	1,385	154
1978	771	97
1979	661	80
1980	419	41
1981	394	24
1982	288	26
1983	264	25
1984	220	25

CHAPTER 4

THE PRICE INDEXES

The price index used as a deflator to convert current-dollar values to constant-dollar values is a Paasche formula index,

$$(1) \qquad I_{o,t} = \frac{\Sigma P_{it} Q_{it}}{\Sigma P_{io} Q_{it}}$$

where, for model i, P_{it} and P_{io} denote prices in the current and base periods, respectively, and Q_{it} denotes the quantity purchased in the current period. The problem encountered in constructing such an index for products experiencing rapid change is that models purchased in the current period may not have existed in the base period.

Matched-model Index

The most frequently used approach for dealing with these problems uses observations only for the models that exist in both period t and in period 0. Models that exist only in the current period are ignored. Such an index may be referred to as a "matched-model" index.

Because models of computing equipment changes so rapidly from one time period to another, it was not possible to calculate a matched-model index using equation (1). Instead, matched models for 2 adjacent years were used to calculate an index where the base period is the first of the 2 years (that is, t-1):

$$(2) \qquad I_{t-1,t} = \frac{\Sigma P_{it} Q_{it}}{\Sigma P_{i,t-1} Q_{it}}$$

An index for the entire period is calculated as a multiplicative "chain" of the adjacent-year indexes:

$$(3) \quad I_{o,t} = I_{o1} \times I_{12} \times \ldots \times I_{t-1,t}$$

The index is referred to as a "chain index of matched models."

The assumption underlying the matched-model procedure is that the mean price change associated with the introduction of new models (or the discontinuance of old ones) equals the mean price change observed for models that are common to both periods. In other words, use of the matched-model procedure assumes that prices of models embodying old technology adjust instantaneously, so that their quality-adjusted prices are equal to those of the models embodying improved technology. If the assumption holds, the price change in the matched models equals the unobserved price change implicit in the introduction of new models (or the discontinuance of old ones). When there is price disequilibrium however, this assumption is invalid; the matched-model index will most likely understate the magnitude of changes in quality adjusted prices.

The Composite Index

The "composite" index uses the matched-model approach whenever models exist in both current and base periods and estimates hypothetical prices for the models that did not exist in the base period from hedonic equations. If an "overlap" model (one that exists in both periods) is

designated "i" and a model present in period t but not in period o is designated "j," then the composite index is:

$$(4) \qquad I_{ot} = \frac{\Sigma P_{it} Q_{it} + \Sigma P_{jt} Q_{jt}}{\Sigma P_{io} Q_{it} + \Sigma \hat{P}_{jo} Q_{jt}}$$

In this formula, $\hat{P}_{jo}$ denotes the estimate, taken from the hedonic equation, or the hypothetical price that the "missing" model would have commanded in the base period. Note that when 1982 is the base (as it is for all the present calculations) and a year subsequent to 1982 is "year t," then P_{jo} is the hypothetical price for a new model. When a year earlier than 1982 (such as 1977) is year t," then P_{jo} is the hypothetical price for a discontinued model.

When the base period is in a state of technological disequilibrium and multiple price regimes are present, some convention must be adopted in estimating P_{jo} because there is more than one price prevailing for any set of model characteristics. In this study, the dominant technology -- that is, the technology class with the greatest value share of shipments in the base period (1982) -- was used to determine the hypothetical price P_{jo}. In 1982, for processors, the majority of models shipped were from technology class 8; embodying 64k memory chips.

The Characteristics Price Index

In hedonic studies, one can identify more than one kind of price. The conventional concept is that of the price of the model. A second concept is that of the prices of the "characteristics." One can use the estimated characteristics prices -- shown in Table 7 -- to construct a price index.

Given the formulation of the hedonic functions, the implicit dollar price of the kth characteristic possessed by the ith model of the mth technology class would be:

$$(5) \qquad \hat{P}_{kimt} = b_k \frac{P_{imt}}{x_{kim}}$$

where b_k is the regression coefficient for the kth characteristic (estimated as constant in equation 2' for all years of the study), x_{kim} denotes the quantity of the kth characteristic possessed by model i, and P_{imt} is the price for model i, of technology class m, at time t.

The characteristics price index is:

$$(6) \qquad I_{ot} = \frac{\Sigma\Sigma\Sigma_{kmi} (bx\ P_{imt})\ (x_{kim}Q_{imt})}{\Sigma\Sigma\Sigma_{kmi} (bx\ P_{imo})\ (x_{kim}Q_{imt})}.$$

where $x_{kim}Q_{imt}$ denotes the quantity of the kth characteristic possessed by model i of the mth technology class in period t. If the technology classes and models within them exist in both period t and in the base period, the characteristics price index would equal the matched-model index in Equation 1.

The Regression Index

The regression index uses no actual prices. It is frequently shown in other studies and is presented here for comparison purposes. It is created directly from the year dummies in the regressions. The price index number for the regression index in Table 8 is based on the combined expression for the regression coefficients for the year dummies and the dominant technology class. Dominant is defined as the technology class whose value share of shipments was highest in each year. It will be truer than an index of "best" (which could be constructed from the year dummies) because it represents products that are widely available.[22] Regression indexes may produce indexes that differ from alternative indexes that use hedonic methods.[23]

Index Comparisons

With the exception of the matched model index, all of the indexes show dramatic 17-20% average annual price declines over the period. As expected, the matched model index understated the magnitude of price reductions in periods of technological innovation and diffusion. During 1982-1984, a period characterized by no new technological introduction, it is comforting to see that changes in the matched model index are close to those in the other indexes.

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[22]The regression could have been reestimated omitting the dominant class in each year rather than "best." The resulting time dummy coefficients are a linear transformations of those estimated with "best" omitted and would yield the same result.

[23]See Triplett and McDonald.

Use in Estimating the Computer Component of the Office, Computing and Accounting Machinery Component of PDE

The composite index, estimated from Equation 2' was combined by the BEA with analogous indexes estimated for storage devices, printers and displays and used in the latest revision of the GNP accounts. Using revised estimates of current dollar purchases of computing equipment and the new deflator, the growth in the constant dollar value of computing equipment for the period 1972-1984 averaged 42.5% per year. This compares with a 22.4% growth rate it would have shown, had the previously published deflator been used.[24]

[24]The previously published deflator had a value of 1 in every period. It had been assumed that price changes were exactly offset by quality changes. This practice had long been recognized as poor, but a replacement was not easily devised.

TABLE 8

PRICE INDEXES
(1982 = 100)

	MATCHED MODELS	REGRESSION	COMPOSITE POOLED TS/CS	COMPOSITE SINGLE YEARS	COMPOSITE CHAR TS/CS
1972	214.1	989.5	834.3	934.5	787.5
1973	214.6	1047.5	865.8	998.5	924.5
1974	219.9	814.2	788.6	847.4	780.0
1975	228.9	792.5	703.7	743.4	721.0
1976	223.6	777.6	665.3	681.6	711.8
1977	183.5	499.3	473.6	527.1	505.3
1978	147.5	262.0	242.0	271.3	283.3
1979	136.4	242.5	204.9	215.9	242.8
1980	115.4	177.0	147.2	146.8	148.0
1981	111.1	113.3	118.6	119.8	125.4
1982	100.0	100.0	100.0	100.0	100.0
1983	89.7	90.6	93.9	86.5	92.7
1984	73.7	77.0	80.8	69.6	80.6
1972-77	-3.0	-12.8	-11.2	-10.8	-8.5
1977-84	-12.2	-23.4	-22.3	-25.1	-23.1
1972-84	-8.5	-19.2	-17.8	-19.5	-17.3

CHAPTER 5

SUMMARY

Expansion of the traditional hedonic model to allow for the presence of technologically induced disequilibrium was developed and estimated. Empirical results indicate that the introduction of new models of computer processors embodying technological improvements, initially creates price disequilibrium. The market for computer processors is rarely observed in equilibrium and full market adjustment takes longer than one year. The market place reacts with the reduction in prices of models embodying older technologies as they continue to be sold until age associated price reductions of the new technology make them unable to maintain their price competitiveness, driving them out of production. With rare exception, disequilibrium was characterized by two price regimes- one for models priced like those embodying "best" technology available and another, higher one priced like those embodying a "nonbest".

Plausibility of the findings is based on the explanation of consumer tolerances of non-quality associated price differences, that is, multiple price regimes, which must be present for transactions to occur at technology driven different supply prices.The path of adjustment is most often observed in the form of continued price reductions of models embodying older technologies as the new one becomes diffused, (widely available) tracing out the workings of a dynamic and competitive marketplace.

The study represents an improvement over other hedonic studies of computing equipment in three ways. The selection of processors, rather than configured systems, provides the basis to estimate quality adjusted price indexes that more closely match an industry's output. The specification of characteristics which more completely account for the capabilities of the equipment in focus enable increased likelihood of full quality adjustment. The expansion of a traditional hedonic model to account for technologically induced disequilibrium is necessary and provides the means to derive useful estimates of prices of unobserved models for the purpose of constructing quality adjusted price indexes without risk of technology induced bias on characteristics' coefficients.

Limitations of the study include small sample size directly resulting from the requirement that the measure of processor speed must be adequate and comparable. The use of list prices rather that transactions prices is a second limitation. It could result in an upward bias in the magnitude of technology class estimated price differentials if models embodying aged "nonbest" technologies are sold at discounted prices.

CHAPTER 6

CONCLUSION

An hedonic model can be useful in estimating quality adjusted price indexes for output of complex products manufactured in an industry characterized by rapid technological change. Three ingredients contributed to its successful application in the case of computer processors: (1) the unit of study closely matches the industry's output, (2) the selected characteristics provide adequate means to measure overall quality in a comparable way, (3) and the model is expanded to allow for the presence of technologically induced disequilibrium which avoids the risk of biased estimates of characteristic coefficients.

The expanded hedonic model is used to derive estimates for missing reference period prices in a quality adjusted price index. This represents an improvement to the alternative matched-model approach which requires market equilibrium in prices -- an assumption which in the case of computer processors is rarely valid. Furthermore, the expanded model also permits for the first time, direct examination of the path of market adjustment back to equilibrium and in the case of processors revealed the workings of a marketplace characterized by rapid change and intense competition.

APPENDIX

EQUATION 1

		SSE	17.290600	F RATIO	413.77
		DFE	281		
DEP VAR: ln(PRICE)		MSE	0.061532	R-SQUARE	0.9537
VARIABLE	DF	PARAMETER ESTIMATE	STANDARD ERROR	T RATIO	
INTERCEPT	1	7.577679	0.080545	94.0802	
LMIPS	1	0.797566	0.022699	35.1365	
LMEM	1	0.172742	0.026348	6.5561	
DUM73	1	0.247558	0.112419	2.2021	
DUM74	1	0.263217	0.107741	2.4431	
DUM75	1	0.053405	0.113390	0.4710	
DUM76	1	-0.019843	0.108893	-0.1822	
DUM77	1	-0.388725	0.109503	-3.5499	
DUM78	1	-0.761353	0.108027	-7.0478	
DUM79	1	-1.062589	0.107190	-9.9132	
DUM80	1	-1.410951	0.106002	-13.3106	
DUM81	1	-1.601752	0.104905	-15.2686	
DUM82	1	-1.737711	0.104821	-16.5779	
DUM83	1	-1.913002	0.106613	-17.9435	
DUM84	1	-2.094333	0.109289	-19.1633	

EQUATION 2

		SSE	9.958698	F RATIO	247.05
		DFE	257		
DEP VAR: ln(PRICE)		MSE	0.038750	R-SQUARE	0.9734
VARIABLE	DF	PARAMETER ESTIMATE	STANDARD ERROR	T RATIO	
INTERCEPT	1	7.945483	0.100405	79.1347	
LMIPS	1	0.780404	0.020006	39.0090	
LMEM	1	0.218943	0.021791	10.0475	
DUM73	1	-0.238623	0.129157	-1.8475	
DUM74	1	-0.195011	0.122238	-1.5953	
DUM75	1	-0.746222	0.174610	-4.2737	
DUM76	1	-0.797988	0.174610	-4.5701	
DUM77	1	-1.002879	0.134351	-7.4646	
DUM78	1	-1.244792	0.134351	-9.2652	
DUM79	1	-2.283200	0.174798	-13.0619	
DUM80	1	-2.257239	0.135341	-16.6782	
DUM81	1	-2.167541	0.122725	-17.6618	
DUM82	1	-2.292601	0.120431	-19.0366	
DUM83	1	-2.391602	0.117703	-20.3190	
DUM84	1	-2.554427	0.121670	-20.9948	
CORE72	1	-0.554157	0.127186	-4.3571	
BP1K73	1	0.294874	0.128023	2.3033	
BP1K74	1	0.283982	0.121088	2.3453	
FET2K75	1	0.523900	0.158340	3.3087	
FET1K76	1	0.159619	0.199764	0.7990	
FET2K76	1	0.557116	0.158340	3.5185	
FET1K77	1	0.318507	0.130192	2.4464	
FET2K77	1	0.382654	0.127528	3.0006	
FET1K78	1	0.378800	0.130192	2.9096	
FET2K78	1	-0.084079	0.113689	-0.7396	
FET2K79	1	0.877286	0.161463	5.4334	
FET4K79	1	0.833202	0.157017	5.3065	
FET2K80	1	0.537243	0.115726	4.6424	
FET4K80	1	0.543794	0.102056	5.3284	
FET2K81	1	0.261775	0.097510	2.6846	
FET4K81	1	-0.037550	0.098922	-0.3796	
F16K81	1	0.326954	0.087536	3.7351	
FET2K82	1	0.147398	0.145683	1.0118	
FET4K82	1	0.142178	0.090941	1.5634	
F16K82	1	0.281465	0.075935	3.7066	
FET2K83	1	0.176058	0.142916	1.2319	
F16K83	1	0.032037	0.086229	0.3715	
F16K84	1	-0.049791	0.061379	-0.8112	

EQUATION 2'

		SSE	10.219432	F RATIO	326.27
		DFE	266		
DEP VAR: ln(PRICE)		MSE	0.038419	R-SQUARE	0.9727
VARIABLE	DF	PARAMETER ESTIMATE	STANDARD ERROR	T RATIO	
INTERCEPT	1	7.943541	0.099875	79.5351	
LMIPS	1	0.782893	0.018910	41.4017	
LMEM	1	0.215084	0.021232	10.1304	
DUM73	1	-0.234675	0.128565	-1.8253	
DUM74	1	-0.191375	0.121667	-1.5729	
DUM75	1	-0.742013	0.173687	-4.2721	
DUM76	1	-0.713853	0.141169	-5.0567	
DUM77	1	-0.996704	0.133588	-7.4610	
DUM78	1	-1.280713	0.120635	-10.6165	
DUM79	1	-2.276428	0.173962	-13.0857	
DUM80	1	-2.248901	0.134552	-16.7140	
DUM81	1	-2.170567	0.117730	-18.4369	
DUM82	1	-2.246169	0.116959	-19.2048	
DUM83	1	-2.371737	0.116153	-20.4191	
DUM84	1	-2.562078	0.118104	-21.6934	
CORE72	1	-0.553615	0.126636	-4.3717	
BP1K73	1	0.292540	0.127453	2.2953	
BP1K74	1	0.281960	0.120558	2.3388	
FET2K75	1	0.523327	0.157411	3.3246	
FET2K76	1	0.476617	0.120637	3.9508	
FET1K77	1	0.317258	0.129382	2.4521	
FET2K77	1	0.381630	0.126958	3.0060	
FET1K78	1	0.419647	0.116036	3.6165	
FET1K79	1	1.178943	0.196806	5.9904	
FET2K79	1	0.877021	0.160694	5.4577	
FET4K79	1	0.832551	0.156193	5.3303	
FET24K80	1	0.540045	0.095372	5.6625	
FET2K81	1	0.272866	0.091740	2.9743	
FET16K81	1	0.337813	0.082057	4.1168	
FET16K82	1	0.242539	0.072299	3.3547	

SINGLE YEAR REGRESSIONS RESULTS

				TECHNOLOGY CLASS											
	CONSTANT	ln(MIPS)	ln(MEM)	1	2	3	4	5	6	7	8	R^2	F	SSE	DF
1972	8.074	.764	.322	-.590	*							.9689	62.4	.696	6
	(37.7)	(3.8)	(2.0)	(-2.6)											
1973	7.559	.553	.266			.149	*					.9831	116.3	.159	6
	(82.6)	(6.3)	(3.4)			(1.3)									
1974	7.614	.668	.212			.243		*				.9837	160.8	.248	8
	(79.8)	(8.6)	(2.8)			(2.1)									
1975	7.293	.726	.200					.358	*			.9934	299.2	.141	6
	(61.6)	(9.8)	(2.7)					(2.4)							
1976	7.247	.750	.173					.406	*			.9938	425.4	.141	8
	(94.2)	(13.7)	(2.9)					(4.7)							
1977	7.176	.698	.145				-.014	.254	*			.9782	101.2	.255	9
	(38.8)	(5.0)	(1.5)				(0.0)	(1.7)							
1978	6.710	.557	.322				.101	**	*			.9822	220.5	.193	12
	(41.5)	(7.3)	(3.1)				(0.5)								
1979	5.626	.560	.185				.867	1.176	1.225		*	.9944	423.6	.008	12
	(59.1)	(10.4)	(3.2)				(7.5)	(12.5)	(11.7)						
1980	5.638	.593	.170					.922	.922		*	.9859	465.3	.326	20
	(57.7)	(9.6)	(3.4)					(7.4)	(7.4)						
1981	5.656	.801	.270					.232	**	.355	*	.9730	261.6	.767	28
	(61.9)	(20.2)	(5.6)					(2.9)		(5.2)					
1982	5.629	.852	.203					**		.294	*	.9600	287.8	1.925	36
	(42.2)	(14.2)	(2.8)							(3.2)					
1983	5.520	.834	.204					**		**	*	.9689	1692.0	.887	45
	(65.9)	(24.1)	(4.6)												
1984	5.261	.813	.235							**	*	.9524	450.0	2.182	45
	(35.5)	(15.0)	(3.4)												

*CLASS PRESENT IN SAMPLE BUT COEFFICIENT OMITTED FROM REGRESSION TO AVOID SINGULAR MATRIX.
**PRESENT IN SAMPLE BUT OMITTED BECAUSE NOT STATISTICALLY DIFFERENT FROM ZERO.

EQUATION 2'

RESTRICTION: COEFFICIENTS ON LMIPS AND LMEM SUM TO 1

		SSE	10.220373	F RATIO	339.16
		DFE	267		
DEP VAR: ln(PRICE)		MSE	0.038279	R-SQUARE	0.9727
	DF	PARAMETER ESTIMATE	STANDARD ERROR	T RATIO	
INTERCEPT	1	7.946551	0.097827	81.2309	
LMIPS	1	0.783340	0.018659	41.9820	
LMEM	1	0.216660	0.018659	11.6116	
DUM73	1	-0.237588	0.126980	-1.8711	
DUM74	1	-0.193328	0.120804	-1.6003	
DUM75	1	-0.747761	0.169450	-4.4129	
DUM76	1	-0.717615	0.138855	-5.1681	
DUM77	1	-1.003138	0.126874	-7.9066	
DUM78	1	-1.286944	0.113668	-11.3219	
DUM79	1	-2.280930	0.171255	-13.3189	
DUM80	1	-2.253646	0.130853	-17.2227	
DUM81	1	-2.176893	0.110374	-19.7229	
DUM82	1	-2.253829	0.106033	-21.2560	
DUM83	1	-2.379826	0.103835	-22.9192	
DUM84	1	-2.570846	0.103785	-24.7709	
CORE72	1	-0.554453	0.126291	-4.3903	
BP1K73	1	0.294793	0.126406	2.3321	
BP1K74	1	0.283254	0.120055	2.3594	
FET2K75	1	0.527121	0.155249	3.3953	
FET2K76	1	0.478425	0.119864	3.9914	
FET1K77	1	0.321218	0.126653	2.5362	
FET2K77	1	0.383272	0.126292	3.0348	
FET1K78	1	0.423404	0.113319	3.7364	
FET1K79	1	1.181669	0.195676	6.0389	
FET2K79	1	0.875313	0.160029	5.4697	
FET4K79	1	0.830412	0.155309	5.3468	
FET24K80	1	0.538008	0.094307	5.7048	
FET2K81	1	0.271733	0.091287	2.9767	
FET16K81	1	0.338303	0.081847	4.1333	
FET16K82	1	0.244088	0.071487	3.4144	
RESTRICTION	-1	-0.465425	2.967945	-0.1568	

EQUATION 2'

TEST OF MEMORY SIZE RULE

		SSE	10.206962	F RATIO	303.31
		DFE	264		
VAR: ln(PRICE)		MSE	0.038663	R-SQUARE	0.9727
VARIABLE	DF	PARAMETER ESTIMATE	STANDARD ERROR	T RATIO	
INTERCEPT	1	7.937632	0.101661	78.0791	
LMIPS	1	0.778486	0.021989	35.4036	
LMEM	1	0.214175	0.023522	9.1054	
LMINMIPS	1	0.018961	0.036081	0.5255	
LMINMEM	1	-0.012370	0.030808	-0.4015	
DUM73	1	-0.228340	0.130858	-1.7449	
DUM74	1	-0.185508	0.123795	-1.4985	
DUM75	1	-0.736839	0.175263	-4.2042	
DUM76	1	-0.706702	0.143732	-4.9168	
DUM77	1	-0.985042	0.139365	-7.0681	
DUM78	1	-1.269083	0.126883	-10.0020	
DUM79	1	-2.263620	0.179688	-12.5975	
DUM80	1	-2.234509	0.143814	-15.5374	
DUM81	1	-2.156646	0.127406	-16.9273	
DUM82	1	-2.231971	0.126729	-17.6121	
DUM83	1	-2.356720	0.126969	-18.5614	
DUM84	1	-2.546587	0.129465	-19.6700	
CORE72	1	-0.552890	0.127063	-4.3513	
BP1K73	1	0.287839	0.128761	2.2355	
BP1K74	1	0.277728	0.121724	2.2816	
FET2K75	1	0.524020	0.157920	3.3183	
FET2K76	1	0.475333	0.121082	3.9257	
FET1K77	1	0.315443	0.129912	2.4281	
FET2K77	1	0.377330	0.127924	2.9496	
FET1K78	1	0.417864	0.116531	3.5859	
FET1K79	1	1.175264	0.197831	5.9407	
FET2K79	1	0.875917	0.161246	5.4322	
FET4K79	1	0.830691	0.156821	5.2971	
FET24K80	1	0.537233	0.096253	5.5815	
FET2K81	1	0.272591	0.092041	2.9616	
FET16K81	1	0.338214	0.082320	4.1085	
FET16K82	1	0.241659	0.072587	3.3292	

EQUATION 2

		SSE	9.958698	F RATIO	240.66
		DFE	257		
DEP VAR: ln(PRICE/ GNP DEFLATOR)		MSE	0.038750	R-SQUARE	0.9727
VARIABLE	DF	STANDARD ESTIMATE	ERROR	T RATIO	
INTERCEPT	1	8.062017	0.100405	80.2954	
LMIPS	1	0.780404	0.020006	39.0090	
LMEM	1	0.218943	0.021791	10.0475	
DUM73	1	-0.277196	0.129157	-2.1462	
DUM74	1	-0.332327	0.122238	-2.7187	
DUM75	1	-0.978759	0.174610	-5.6054	
DUM76	1	-1.089316	0.174610	-6.2386	
DUM77	1	-1.356064	0.134351	-10.0934	
DUM78	1	-1.671014	0.134351	-12.4377	
DUM79	1	-2.801191	0.174798	-16.0253	
DUM80	1	-2.869079	0.135341	-21.1989	
DUM81	1	-2.863493	0.122725	-23.3326	
DUM82	1	-3.053617	0.120431	-25.3557	
DUM83	1	-3.192242	0.117703	-27.1213	
DUM84	1	-3.388801	0.121670	-27.8525	
CORE72	1	-0.554157	0.127186	-4.3571	
BP1K73	1	0.294874	0.128023	2.3033	
BP1K74	1	0.283982	0.121088	2.3453	
FET2K75	1	0.523900	0.158340	3.3087	
FET1K76	1	0.159619	0.199764	0.7990	
FET2K76	1	0.557116	0.158340	3.5185	
FET1K77	1	0.318507	0.130192	2.4464	
FET2K77	1	0.382654	0.127528	3.0006	
FET1K78	1	0.378800	0.130192	2.9096	
FET2K78	1	-0.084079	0.113689	-0.7396	
FET2K79	1	1.181272	0.197680	5.9757	
FET2K79	1	0.877286	0.161463	5.4334	
FET4K79	1	0.833202	0.157017	5.3065	
FET2K80	1	0.537243	0.115726	4.6424	
FET4K80	1	0.543794	0.102056	5.3284	
FET2K81	1	0.261775	0.097510	2.6846	
FET4K81	1	-0.037550	0.098922	-0.3796	
F16K81	1	0.326954	0.087536	3.7351	
FET2K82	1	0.147398	0.145683	1.0118	
FET4K82	1	0.142178	0.090941	1.5634	
F16K82	1	0.281465	0.075935	3.7066	
FET2K83	1	0.176058	0.142916	1.2319	
F16K83	1	0.032037	0.086229	0.3715	
F16K84	1	-0.049791	0.061379	-0.8112	

EQUATION 2'

		SSE	10.219432	F RATIO	317.83
		DFE	266		
DEP VAR: ln(PRICE/ GNP DEFLATOR)		MSE	0.038419	R-SQUARE	0.9720
	DF	PARAMETER ESTIMATE	STANDARD ERROR	T RATIO	
INTERCEPT	1	8.060075	0.099875	80.7019	
LMIPS	1	0.782893	0.018910	41.4017	
LMEM	1	0.215084	0.021232	10.1304	
DUM73	1	-0.273248	0.128565	-2.1254	
DUM74	1	-0.328691	0.121667	-2.7016	
DUM75	1	-0.974550	0.173687	-5.6110	
DUM76	1	-1.005180	0.141169	-7.1204	
DUM77	1	-1.349889	0.133588	-10.1049	
DUM78	1	-1.706935	0.120635	-14.1496	
DUM79	1	-2.794419	0.173962	-16.0634	
DUM80	1	-2.860741	0.134552	-21.2612	
DUM81	1	-2.866519	0.117730	-24.3483	
DUM82	1	-3.007184	0.116959	-25.7115	
DUM83	1	-3.172378	0.116153	-27.3121	
DUM84	1	-3.396452	0.118104	-28.7582	
CORE72	1	-0.553615	0.126636	-4.3717	
BP1K73	1	0.292540	0.127453	2.2953	
BP1K74	1	0.281960	0.120558	2.3388	
FET2K75	1	0.523327	0.157411	3.3246	
FET2K76	1	0.476617	0.120637	3.9508	
FET1K77	1	0.317258	0.129382	2.4521	
FET2K77	1	0.381630	0.126958	3.0060	
FET1K78	1	0.419647	0.116036	3.6165	
FET1K79	1	1.178943	0.196806	5.9904	
FET2K79	1	0.877021	0.160694	5.4577	
FET4K79	1	0.832551	0.156193	5.3303	
FET24K80	1	0.540045	0.095372	5.6625	
FET2K81	1	0.272866	0.091740	2.9743	
FET16K81	1	0.337813	0.082057	4.1168	
FET16K82	1	0.242539	0.072299	3.3547	

EQUATION 3

		SSE	46.076808	F RATIO	400.61
		DFE	290		
DEP VAR:	ln(PRICE/ GNP DEFLATOR)	MSE	0.158886	R-SQUARE	0.8735
VARIABLE	DF	PARAMETER ESTIMATE	STANDARD ERROR	T RATIO	
INTERCEPT	1	7.976121	0.091866	86.8235	
LMIPS	1	0.756705	0.036502	20.7303	
LMEM	1	0.127871	0.042136	3.0348	
LMT	1	-0.165251	0.028724	-5.7531	
MEMAGE	1	-0.091202	0.017945	-5.0823	
DLLMB	1	-0.383965	0.034203	-11.2260	

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